REMARKS

Attorney Docket Number:

Applicant requests that the attorney docket number be amended to be 024299-0352.

Status Of Claims:

New claims 25-32 have been added. Thus, claims 1-32 are present for examination.

Prior Art Rejection:

Claims 1-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Andreas (Pub. No. US 2004/0093450).

With respect to claims 1-24, as amended, the rejection is respectfully traversed.

Independent claim 1, as amended, recites an electronic device comprising:

> "a controller programmed to produce first address data on an output thereof;
> a plurality of integrated circuits (ICs) addressable by the controller; and
> a shared bus joining the controller and the plurality of ICs;
> wherein each of the ICs comprises an input for receiving address data representing an address of the IC on the shared bus, and an output for providing modified address data different from the received address data, and
> wherein the input of a first IC communicates with the output of the controller and the inputs of succeeding ICs communicate with the outputs of preceding ICs in a daisy chain configuration." (Emphasis Added)

The electronic device including the above-quoted features has the advantage that a controller produces a first address for a first IC, and each IC has an input for receiving address data representing an address of the IC and an output for providing modified address data to a succeeding IC in a daisy chain configuration. Thus, each IC in the daisy chain is provided with an address. Each IC then uses its address to distinguish whether or not a communication on the shared bus is intended for that IC. (see Specification page 1, lines 23-24; page 2, lines 20-26; page 5, lines 1-11).

Andreas neither discloses nor suggests the electronic device including the above-quoted features with each IC having an input for receiving address data representing an address of the IC and an output for providing modified address data to a succeeding IC in a daisy chain configuration. In Andreas, the Serial Device Slaves are never assigned an address. Instead, in Andreas, a Serial Bus Master sends a mask value to the first Serial Device Slave in a daisy chain configuration. (Andreas; abstract; paragraph [0030], [0036]). The mask value is serially clocked by the first Serial Device Slave and is sent to the next Serial Device Slave in the daisy chain. (Andreas; paragraph [0036]). Each serial device treats the kth bit clocked through it as its corresponding mask value portion. (Andreas; paragraph [0036]). If the bit is "1" then the device is enabled, but if "0" then the device is disabled. (Andreas; paragraph [0040]).

Because the Serial Bus Master in Andreas uses a mask value instead of assigning an address to each IC, the Serial Bus Master in Andreas cannot issue commands on a shared bus and have the ICs distinguish whether or not the command has been issued to them. The device in Andreas requires that a mask value be serially clocked through each Serial Device Slave every time a command is issued to a different Serial Device Slave. (Andreas; Figure 3, reference 390; Figure 4, reference 440; paragraph [0035]). Thus, as shown in Andreas by the flowchart of Figure 4, when operating in the daisy chain mode, the mask value must be clocked in to be received by each Serial Device Slave before responding to each command. (Andreas; Figure 4, references 430, 440, 450, 460).

As a result, with the clocked mask value of Andreas, a set number of clock cycles are required to transfer the mask value to each Serial Device Slave in the daisy chain, which leads to time being spent just to exchange the mask value before each command. For example, as shown in Figure 3 of Andreas, 8 clock cycles are required to transfer a mask value of 8 bits to each Serial Device Slave before each command. (Andreas; Figure 3, reference 380). In contrast, the electronic device including the above-quoted features does not require time to transfer a mask value between ICs before each command, because each IC is provided with an address and then

the ICs can all determine at the same time whether a command on a shared bus is addressed to them.

Furthermore, claim 1 has been amended to clarify that each IC provides as output modified address data different from the received address data. The Serial Device Slaves in Andreas do not modify the mask value that they receive, but output the same mask value that they receive. (Andreas; Figure 3; paragraph [0036]) The specification in Andreas states that "the SDI THRU signal for a device should be the same as the clocked SDI signal for that device while the mask value is being distributed." (Andreas; paragraph [0036])(Emphasis Added). Because the mask signal is not modified in Andreas by the Serial Device Slaves, only k serial devices may be uniquely specified using a k-bit mask value. (Andreas; paragraph [0040]). In contrast, embodiments of the electronic device of claim 1 can specify up to 2^k unique addresses with a k-bit address because the address can be modified by each IC before being output to a succeeding IC. For example, with a 4 bit address, sixteen ICs could be uniquely addressed. (see Specification page 2, lines 2-4).

The Examiner points to Andreas, paragraphs [0023-0026] as disclosing ICs comprising "an input for receiving address data representing an address of the IC on the shared bus". (Emphasis Added). Andreas discloses in paragraph [0025] that a "command word includes a plurality of address bits A0-A6 and a R/W bit to indicate whether a read or write operation is to be performed on the indicated address." (Emphasis Added). However, the address bits that are disclosed in Andreas do not represent an address of an IC on a shared bus. Instead, the address bits are used by an IC to perform a command at an address, such as a read or write, after the IC has been enabled by a mask value. (Andreas; paragraph [0021], [0025], [0037]).

Therefore, independent claim 1 is neither disclosed nor suggested by the cited prior art and, hence, is believed to be allowable.

Independent claim 8, as amended, recites an electronic device similar to the electronic device of claim 1 and, thus, is believed to be allowable for at least the same reasons that claim 1 is believed to be allowable.

Independent claim 9, as amended, recites a method for initializing addresses of a plurality of integrated circuits similar to the operation of the electronic device of claim 1 and, thus, is believed to be allowable for at least the same reasons that claim 1 is believed to be allowable.

Independent claim 11 recites an electronic device comprising:

> "a controller;
> a plurality of integrated circuits (ICs) addressable by the controller; and
> a shared bus joining the controller and the plurality of integrated circuits;
> wherein the controller is programmed to produce a series of addresses on the shared bus and to produce an enable signal on an output in conjunction with a first address of the series of addresses,
> wherein each of the ICs comprises an input for receiving an enable signal and an output for providing an enable signal in conjunction with a change in address data on the shared bus, and means for storing an address present on the shared bus as an address of the IC in response to receiving an enable signal, and
> wherein the input of a first IC communicates with the output of the controller and the inputs of succeeding ICs communicate with the outputs of preceding ICs in a daisy chain configuration." (Emphasis Added)

The electronic device including the above-quoted features has the advantage that a controller can produce a series of addresses on a shared bus line and each IC can store an address that is present on the shared bus line upon receiving an enable signal through a daisy chain configuration. Also, each IC comprises an output for providing an enable signal in conjunction with a change in address data on the shared bus. Such a configuration allows for IC addresses to be distributed over a shared bus while ensuring that each IC receives the correct address from the shared bus. (see Specification page 2, line 26 to page 3, line 4; page 6, lines 7-22).

Andreas neither discloses nor suggests the electronic device including the above-quoted features with IC addresses being distributed over a shared bus from a controller and ICs

comprising outputs for providing an enable signal in conjunction with a change in address on the shared bus.

First, as described above with respect to claim 1, the Serial Bus Master in Andreas distributes a mask value before each command and not an address of an IC. (Andreas; paragraph [0030]). Thus, the discussion above with respect to the mask value not being an address of an IC applies also to claim 11 as well.

Second, the Serial Bus Master in Andreas does not even produce the mask value on a shared bus. In fact, Andreas specifically states that "[t]he SDI signal is not part of the shared communication bus 260." (Emphasis Added)(Andreas; paragraph [0026]; Figure 2, references 260, 222). Instead, when the device in Andreas operates in a daisy chain configuration, the SDI input for any serial device is provided by the SDI THRU output of a preceding device in the chain. Thus, the mask value is serially clocked from one Serial Device Slave to the next in the daisy chain in a sequential manner and is not sent on a shared bus. (Andreas; Figure 3, reference 310, 332; paragraph [0036]). Indeed, the operation of the device in Andreas relies on the fact that each Serial Device Slave clocks the mask value before sending the mask value to the next Serial Device Slave in the chain. (Andreas; Figure 3; paragraph [0036]).

Third, the Serial Device Slaves in Andreas do not comprise an output for providing an enable signal in conjunction with a change in address data on a shared bus. As discussed above, when operating in a daisy chain configuration, the apparatus in Andreas does not even have a shared bus on which to send a mask value. (Andreas; Figure 2; paragraph [0026], [0036]). Furthermore, the Serial Device Slaves in Andreas never provide an enable signal that is separate from address data. The Serial Device Slaves do receive a chip select signal, but that signal is output from the Serial Bus Master. (Andreas; Figure 2, reference 170).

Fourth, the Serial Device Slaves in Andreas never store an address present on a shared bus as an address of the Serial Device Slaves. The Serial Device Slaves do store bits of a mask value that is sent before each command, but do not store an address. (Andreas; paragraph

[0041]). Thus, the bits that are stored by the Serial Device Slaves in Andreas can change with each mask value that is sent. (Andreas; paragraph [0036]).

Therefore, independent claim 11 is neither disclosed nor suggested by the cited prior art and, hence, is believed to be allowable.

Independent claim 20 recites an electronic device similar to the electronic device of claim 11 and, thus, is believed to be allowable for at least the same reasons that claim 11 is believed to be allowable.

Independent claim 21 recites a method for initializing addresses of a plurality of integrated circuits similar to the operation of the electronic device of claim 11 and, thus, is believed to be allowable for at least the same reasons that claim 11 is believed to be allowable.

The dependent claims are deemed allowable for at least the same reasons indicated above with regard to the independent claims from which they depend.

Conclusion:

Applicant believes that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 50-0872. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 50-0872. If any extensions of time are needed for timely acceptance of papers

submitted herewith, Applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 50-0872.

Respectfully submitted,

Date October 8, 2004 By _____

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